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Data Processing Patent Eligibility: Federal Circuit Finds Claims Eligible in KPN v. Gemalto

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On November 15, 2019, the Federal Circuit issued an opinion in *Koninklijke KPN N.V. v. Gemalto M2M GmbH et al.*, 2018-1863, that provides additional guidance on the patentability of data processing-related claims. The decision also distinguishes several cases in which claims were found to be ineligible, and helps delineate where the line for subject matter eligibility falls.

KPN had asserted U.S. Patent No. 6,212,662 ("the '662 Patent") which was directed to a device for improved error checking in data transmission systems. The '662 Patent explains that prior error checking systems were vulnerable to some "systematic errors," or repeated errors that prior art error checking algorithms are unable to detect. For example, given a block of data (e.g. "1…0"), a simple error checking system may compare the first and last bits and, identifying that they're different, add a parity bit of 1. However, if the communication system is subject to a systematic error that changes both the first and last bit of the data (e.g. to "0…1", such as might result from a poorly timed transmitter that starts late and ends early), the simple error checking system would not be able to detect the error (because the bits are still different and the parity bit is the same). If the same error is repeated across a number of packets, the system may continue to generate incorrect parity data and the error may persist.

The invention of the '662 Patent varies the error checking algorithm between packets such that while an error may go undetected for a first packet, the same error would be detected in a second packet, as the varied algorithm would not be vulnerable to that particular type of error. The particular implementation claimed by the '662 Patent involved applying a permutation of bits in a data block. As described by the Federal Circuit:

> One example of a permutation may involve the following: "bit 1 to position 2, bit 2 to position 4, bit 3 to position 1 and bit 4 to position 3."… Based on this permutation, a data block of "1100" would transform into "0101." (internal citation omitted)

The district court found claims 1-4 of the '662 Patent directed to the (patent ineligible) abstract idea of "reordering data and generating additional data," analogizing the claims to those at issue in a

litany of Federal Circuit cases: *Two-Way Media Ltd. v. Comcast Cable Communications, LLC*, 874 F.3d 1329 (Fed. Cir. 2017); *RecogniCorp, LLC v. Nintendo Co.*, 855 F.3d 1322(Fed. Cir. 2017); *Intellectual Ventures I LLC v. Capital One Financial Corp.*, 850 F.3d 1332 (Fed. Cir. 2017); and *Digitech Image Technologies, LLC v. Electronics for Imaging, Inc.*, 758 F.3d 1344(Fed. Cir. 2014). In particular, the district court complained that the claims did "not say how data is reordered, how to use reordered data, how to generate additional data, how to use additional data, or even that any data is transmitted," and that the claims did "not say how the permutations are modified in time or modified based on the data."

On appeal to the Federal Circuit, KPN sought reversal as to dependent claims 2-4, but not with respect to independent claim 1. Accordingly, the Federal Circuit's decision did not address claim 1. However, the opinion nevertheless suggests that the differences between claim 1 and 2 form a dividing line for the purposes of patent eligibility.

Specifically, Claim 1 of the '662 Patent (ineligible, and not appealed) recites:

> 1. A device for producing error checking based on original data provided in blocks with each block having plural bits in a particular ordered sequence, comprising:
>
> a generating device configured to generate check data; and
>
> a varying device configured to vary original data prior to supplying said original data to the generating device as varied data;
>
> wherein said varying device includes a permutating device configured to perform a permutation of bit position relative to said particular ordered sequence for at least some of the bits in each of said blocks making up said original data without reordering any blocks of original data.

Eligible claim 2 recites (eligible claims 3-4 depend on claim 2):

> 2. The device according to claim 1, wherein the varying device is further configured to *modify* the permutation *in time*. (emphasis original to Federal Circuit opinion)

In finding claims 2-4 eligible, the Federal Circuit stated that "[b]y requiring that the permutation applied to original data be modified 'in time,' claim 2, which is incorporated into all appealed claims, recites a specific implementation of varying the way check data is generated that improves the ability of prior art error detection systems to detect systematic errors." This limitation thus provided a solution to the problem in the art identified in the '622 Patent. By contrast, claim 1 did not require such varying of the permutation, and could result in the same permutation being applied identically to every packet, which would result in vulnerability to systematic errors and fail to achieve the solution of the specification.

The opinion leans heavily on the specification, which is an important takeaway for practitioners: a

patent that describes a problem in the art and subsequently claims a solution (rather than just the desired result) will be significantly stronger against challenge on the grounds of patent eligibility. For example, the court stated "the claims do not simply recite, without more, the mere desired result of catching previously undetectable systematic errors, but rather recite a specific solution for accomplishing that goal—i.e., by varying the way check data is generated by modifying the permutation applied to different data blocks" (emphasis added). This focus on implementation, rather than a result, is one of the more consistent pieces of guidance from the Federal Circuit, appearing in decisions finding claims both eligible and ineligible. For example, in *Uniloc USA v. ADP,* 2018-1132 at 19 (May 24, 2019), the Federal Circuit found a claim to be ineligible, stating that the patent owner's "attempt to reframe the claimed improvement to allow client-independent user-specific application access must fail; neither that functionality nor how that can be achieved is in the claims." (emphasis added). Similarly, in *Reese v. Sprint*, 2018-1971 at 10 (June 10, 2019), the Federal Circuit found claims to be ineligible, stating that "the claims recite functional language lacking any requirements for how the desired result is achieved" (internal citation omitted). Judge Bryson further emphasized this point in his dissent in *Bridge and Post v. Verizon Communications*, 2018-1697 at 23 (July 5, 2019), stating:

> The distinction between claims that recite functions or results (the "what it does" aspect of the invention) and those that recite concrete means for achieving particular functions or results (the "how it does it" aspect of the invention) is an important indicator of whether a claim is directed to an abstract idea. (emphasis added)

Finally, the Federal Circuit dismissed an argument by Gemalto that the claims were ineligible because they didn't recite a final step of using the check data to detect errors. This argument is similar to the situations in *Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 566 U.S. 66 (2012) and *Vanda Pharmaceuticals Inc. v. West-Ward Pharmaceuticals*, 887 F.3d 1117 (Fed. Cir. 2018). The ineligible claims at issue in *Mayo* recited administering a drug, and determining whether the level of the drug needed to be increased or decreased in subsequent dosages, while the eligible claims at issue in *Vanda* included a post-solution step of actually administering a drug in a modified dosage. Here, the appellee argued that without a post-solution step of performing error checking on real data, the claims were ineligible for the same reasons as in *Mayo*.

The Federal Circuit disagreed, describing how "[a] claim that is directed to improving the functionality of one tool (e.g., error checking device) that is part of an existing system (e.g., data transmission error detection system) does not necessarily need to recite how that tool is applied in the overall system (e.g., perform error detection) in order to constitute a technological improvement that is patent-eligible. Rather, to determine whether the claims here are non-abstract, the more relevant inquiry is 'whether the claims in th[is] patent[] focus on a specific means or method that improves the relevant technology or are instead directed to a result or effect that itself is the abstract idea and merely invoke processes and machinery.'" (emphasis added).

KPN v. Gemalto provides a good guide for patent attorneys working with patents related to data processing. Practitioners should focus on whether the claims recite specific implementation steps (the "how it does it" aspect) that solve a problem identified in the specification, rather than merely stating a result to be achieved (the "what it does" aspect). If a patent claim can be drafted by a person with an understanding of the problem and a desire to solve it but with no knowledge of how to implement the solution (such as a claim that recites providing a desired output, with no recited details

for generating that output), it may be difficult to preserve its eligibility in court.

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